AMENDMENTS

In the Claims

The following is a marked-up version of the claims with the language that is underlined ("___") being added and the language that contains strikethrough ("~~___~~") being deleted:

1 – 14. (Canceled)

15. (Currently Amended) A transmission signal integrity supervisor within an analog front end (AFE), wherein the transmission signal integrity supervisor is configured to detect anomalous conditions and protect the AFE, the transmission signal integrity supervisor comprising:

a clock detector configured to receive a clock signal input and generate a first output signal in response to an at least one clock signal input anomalous condition, wherein the clock detector is further configured to forward the first output signal to at least one of control logic and devices external to the ~~AFE;~~ AFE, the clock detector including a resistor-capacitor combination coupled to a current mirror, the resistor-capacitor combination configured such that the first output signal triggers in response to a clock signal input that falls below a minimum frequency; and

a data supervisor configured to receive a digital data stream and generate a second output signal in response to an at least one digital data stream anomalous condition, wherein the data supervisor is further configured to forward the second output signal to at least one of a line driver within the AFE and devices external the AFE.

16. (Previously Presented) The signal integrity supervisor of claim 15, wherein the first output signal is a reset signal.

17. (Previously Presented) The signal integrity supervisor of claim 15, wherein the second output signal is a power down signal.

18. (Previously Presented) The signal integrity supervisor of claim 15, wherein the data supervisor receives a digital data stream from a delta-sigma modulator.

19. (Previously Presented) The signal integrity supervisor of claim 15, wherein the clock detector comprises a first monostable circuit coupled to a second monostable circuit.

20. (Currently Amended) The signal integrity supervisor of claim 19, wherein the clock detector further ~~comprises: a~~ includes the current ~~mirror; and a~~ mirror and the resistor-capacitor combination is coupled to the current mirror, the resistor-capacitor combination having a resistance and a capacitance value ~~respectively, selected such that the first output signal triggers in response to a clock signal input that falls below a minimum frequency.~~ respectively.

21. (Previously Presented) The signal integrity supervisor of claim 15, wherein the data supervisor comprises:

a comparator; and

a maximum number counter coupled to the comparator.

22. (Previously Presented) The signal integrity supervisor of claim 21, wherein the comparator is configured to compare a data value from a previous clock cycle with a current data value and to generate a reset signal in response to consecutive data levels that vary.

23. (Previously Presented) The signal integrity supervisor of claim 22, wherein the maximum number counter is configured to increment upon detecting a clock cycle until it

receives the reset signal from the comparator.

24. (Previously Presented) The signal integrity supervisor of claim 23, wherein the maximum number counter is configured to generate an output signal upon reaching a maximum count.

25. (Previously Presented) The signal integrity supervisor of claim 24, wherein the maximum number counter comprises a 4-bit asynchronous counter.

26. (Currently Amended) A circuit, comprising:

means for monitoring a digital data stream, wherein the means for monitoring a digital data stream comprises a signal integrity supervisor; and

means for generating an output signal in response to an anomalous condition in the digital data stream, the output signal including a fault recovery response to reset at least one component when the anomalous condition is detected, wherein the means for generating an output signal is responsive to a digital data stream having a number of consecutive data values of equal magnitude wherein the number of consecutive data values reaches a predetermined maximum value.

27. (Previously Presented) The circuit of claim 26, wherein the anomalous condition in the digital data stream creates a direct current (DC) transmit signal.

28. (Canceled)

29. (Previously Presented) The circuit of claim 26, wherein the signal integrity supervisor comprises a clock detector and a data supervisor.

30. (Canceled)

31. (Previously Presented) The circuit of claim 26, wherein the means for generating an output signal is responsive to a digital data stream having a clock signal that falls below a predetermined minimum frequency.

32. (Currently Amended) A transmission unit, comprising:

a signal integrity supervisor configured to generate a response to a digital data stream having an anomalous condition, the signal integrity supervisor further configured to forward the response to ~~at least one of~~ the following:

control logic configured to reset the transmission unit, and

a line driver within the transmission unit, wherein the response powers down the line driver.

33. (Previously Presented) The transmission unit of claim 32, wherein the digital data stream anomalous condition is a clock signal frequency that falls below a predetermined minimum value.

34. (Previously Presented) The transmission unit of claim 32, wherein the digital data stream anomalous condition is a data signal having a corresponding data value that does not vary for a predetermined maximum number of clock cycles.

35. (Previously Presented) The signal integrity supervisor of claim 15, further comprising a delta-sigma modulator coupled to the clock detector and the data supervisor.

36. (Previously Presented) The signal integrity supervisor of claim 35, wherein the delta-sigma modulator is configured to provide at least one of the following: digital-to-analog conversion and analog-to-digital conversion.

37. (Previously Presented) The transmission unit of claim 32, wherein the signal integrity supervisor includes a clock detector configured to receive a clock signal input and generate a first output signal in response to an at least one clock signal input anomalous condition, wherein the clock detector is further configured to forward the first output signal to at least one of control logic and devices external to the AFE.

38. (Previously Presented) The transmission unit of claim 37, wherein the signal integrity supervisor includes a data supervisor configured to receive a digital data stream and generate a second output signal in response to an at least one digital data stream anomalous condition, wherein the data supervisor is further configured to forward the second output signal to at least one of a line driver within the AFE and devices external the AFE.